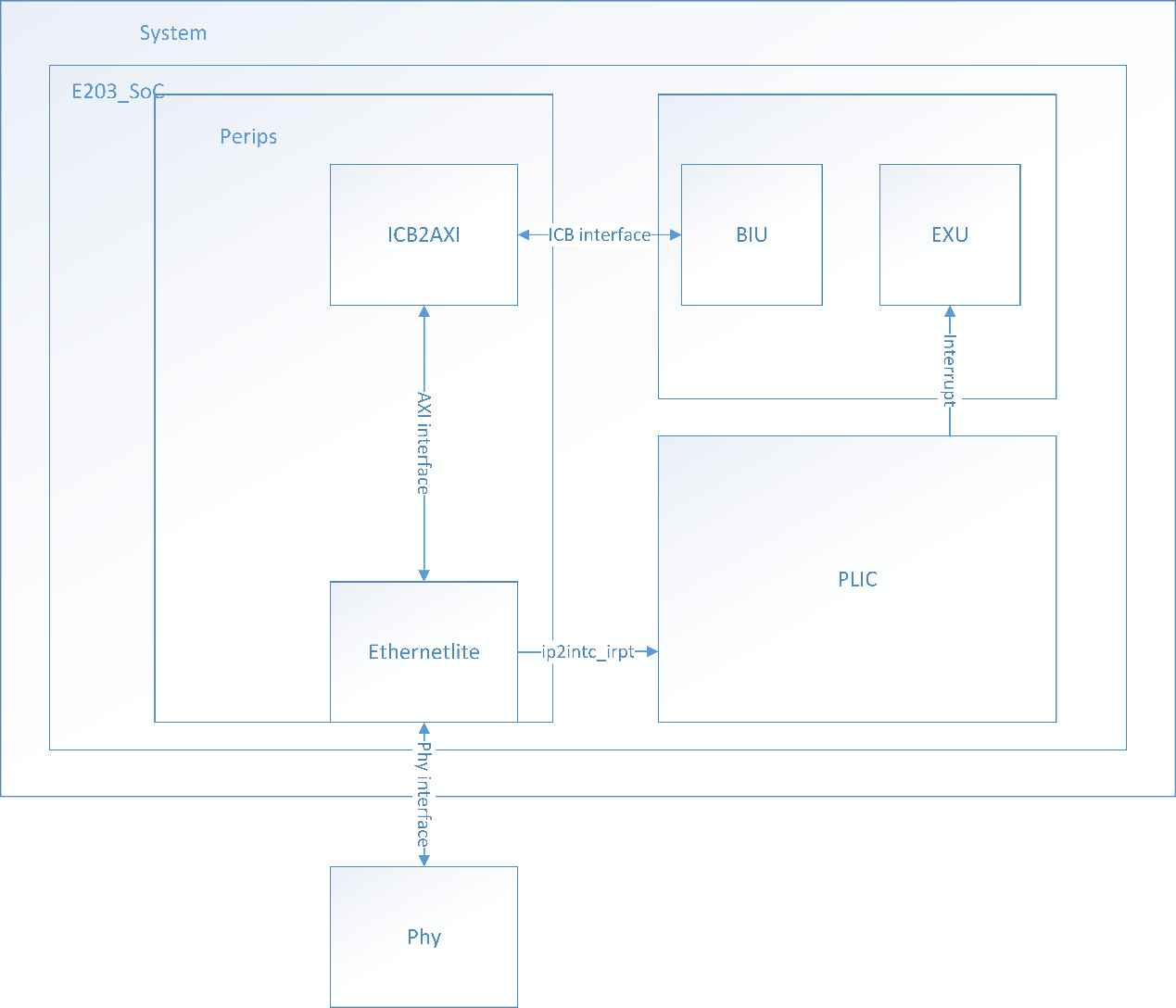
EthernetLite Specification

## 功能介绍

完成以太网的数据链路层功能。对外通过MII接口结合物理层phy芯片通信，对内通过ICB总线和cpu的IP层软件协议进行通信。并能够产生中断信号被PLIC模块接收。

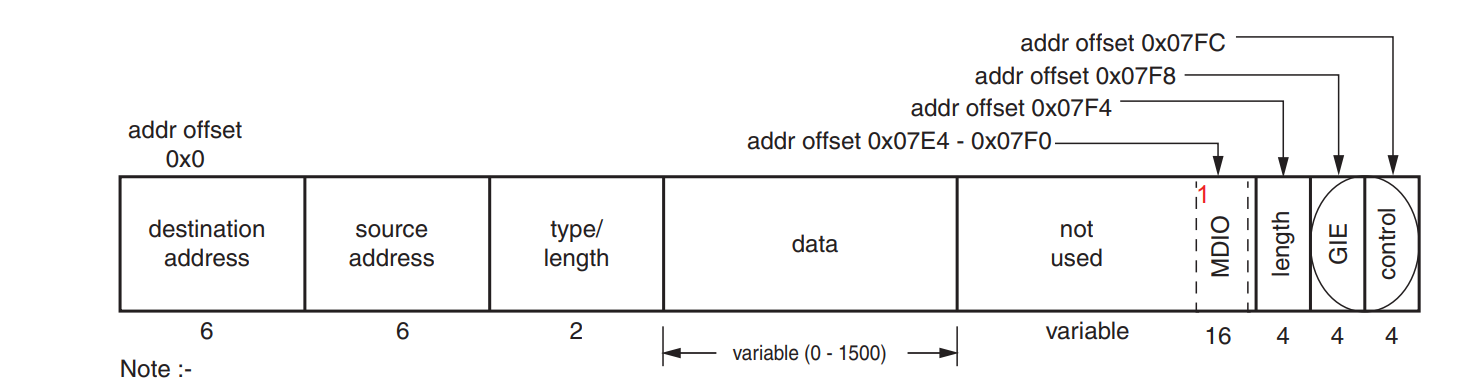


## IO定义

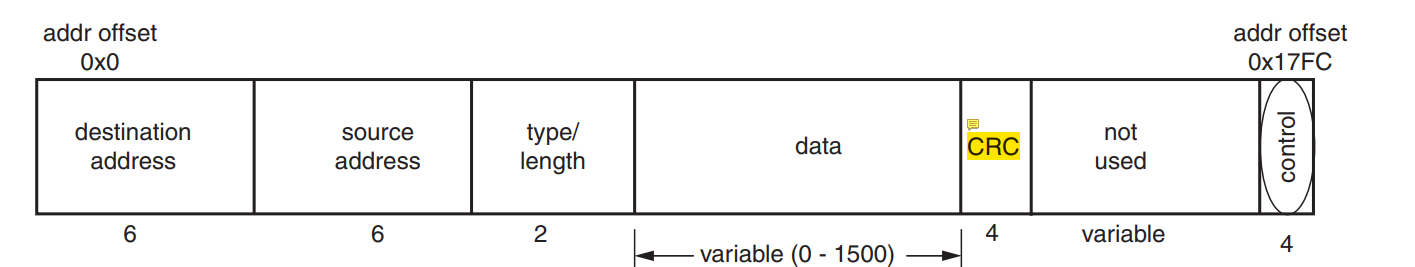
|  |  |  |  |
| --- | --- | --- | --- |
| Name | Direction | Bits | Description |
| Cmd\_valid | I | 1 | 主设备发送读写请求 |
| Cmd\_ready | O | 1 | 从设备返回读写接收信号 |
| Cmd\_read | I | 1 | 读或者写操作指示 |
| Cmd\_addr | I | 32 | 读写地址 |
| Cmd\_wdata | I | 32 | 写操作数据 |
| Cmd\_wmask | I | 3 | 写操作字节掩码 |
| Rsp\_valid | O | 1 | 从设备发送读写反馈请求信号 |
| Rsp\_ready | I | 1 | 主设备返回读写反馈接收信号 |
| Rsp\_rdata | O | 32 | 读反馈数据 |
| ip2intc\_irpt | O | 1 | 上升沿触发的中断信号 |
| Phy\_tx\_clk | I | 1 | 发送时钟来自phy芯片 |
| Phy\_rx\_clk | I | 1 | 接收时钟来自phy芯片 |
| Phy\_rx\_data | I | 4 | 来MII接口的接收数据 |
| Phy\_tx\_data | O | 4 | 向MII接口发送的数据 |
| Phy\_dv | I | 1 | 接收数据有效 |
| Phy\_rx\_er | I | 1 | 接收数据出错 |
| Phy\_tx\_en | O | 1 | 发送数据使能 |
| Phy\_mdc | O | 1 | MDIO接口时钟 |
| Phy\_mdio\_i | I | 1 | MDIO接口输入数据 |
| Phy\_mdio\_o | O | 1 | MDIO接口发送数据 |
| Phy\_mdio\_t | O | 1 | MDIO接口使能输出 |

## 地址映射

发送缓冲区是从0x1500\_0000到0x1500\_07FF的位置



接收缓冲区是从0x1500\_1000到0x1500\_17FF 的位置



寄存器表

|  |  |  |
| --- | --- | --- |
| **Address Offset** | **Register Name** | **Description** |
| 1500\_07E4h | MDIOADDR (1) | MDIO address register |
| 1500\_07E8h | MDIOWR (1) | MDIO write data register |
| 1500\_07ECh | MDIORD (1) | MDIO read data register |
| 1500\_07F0h | MDIOCTRL (1) | MDIO control register |
| 1500\_07F4h | TX Ping Length | Transmit length register for ping buffer |
| 1500\_07F8h | GIE | Global interrupt register |
| 1500\_07FCh | TX Ping Control | Transmit control register for ping buffer |
| 1500\_0FF4h | TX Pong Length (2) | Transmit length register for pong buffer |
| 1500\_0FFCh | TX Pong Control (2) | Transmit control register for pong buffer |
| 1500\_17FCh | RX Ping Control | Receive control register for ping buffer |
| 1500\_1FFCh | RX Pong Control (3) | Receive control register for pong buffer |